Ensemble® 6000 Series OpenVPX™ Intel 4th Generation Core i7 module

4th Generation Intel® Quad-Core™ i7 LDS module with CPU on-die GPU, upgradeable POET™ data plane interface and mezzanine sites



- 4th Generation Intel® Quad-Core™ i7 processor (Haswell mobile class) with AVX2 and on-die GT2 GPU for demanding data/graphics processing
- One XMC and one XMC/PMC mezzanine sites
- 6U OpenVPX[™] compliant VITA 65/46/48 (VPX-REDI) module
- Integrated Gen3 PCIe switching infrastructure for on-board and off-board co-processing

The Ensemble® 6000 Series OpenVPX™ with 4th Generation Intel® Quad-Core™ i7 processor (Haswell mobile class) LDS6525 module from Mercury Systems combines a powerful mobile-class Quad-Core Intel processor, firmware upgradable FPGA implemented switched fabrics for unsurpassed fabric data rates, and configurable mezzanine I/O in a single 6U OpenVPX slot. The LDS6525, as Mercury's latest low-density server, provides a next-generation architecture that balances the computational capabilities of the AVX2-enabled Core i7 processor with Gen 2 Serial RapidIO™ or 10 Gigabit Ethernet data paths. The combination provides a powerful and scalable computing architecture that is well aligned with high-end radar, electronic warfare and image processing applications.

Intel 4th Generation Core i7 Haswell Mobile-Class Processor

At the heart of the LDS6525 is the Intel 64-bit 4th Generation Core i7-4700EQ processor, running at up to 2.4 GHz. This processor includes Advanced Vector Extensions-2 (AVX2) instruction set which doubles the width of the processor's SIMD engine from 128 bit to 256 bit, and includes Fused Multiply-Add (FMA), delivering a significant improvement in floating-point processing.

The 4700EQ includes a large 6 MB cache shared between the cores, allowing many high-performance calculations to remain cache resident. This accelerates processing by eliminating the potential latency required to access DRAM to fetch upcoming data. The processor supports dual high speed DDR3-1600 memory controllers, providing up to 25 GB/s of raw memory bandwidth. 8 GB of DDR3-DRAM with ECC support is populated on the LDS6525.

The four processor cores are supported by the latest on-die GT2 GPU for high definition graphical and intensive parallel data processing. Programming options include the device's native OpenCL support and the efficiency of Intel's FMA.

POET Switched Fabric Interconnect Technology

Mercury's Protocol Offload Engine Technology (POET™) delivers the highbandwidth, low-latency performance of switched fabrics, providing the breadth necessary to eliminate data starvation and to fully utilize the upgraded processing power of Intel 4th Generation Core i7 technology.

The LDS6525 POET instantiation supports the high-bandwidth, low latency, Gen 2 Serial RapidIO switched fabric and 10Gigabit Ethernet protocols. Upgrading the data plane protocol is as simple as loading a new POET image into the local FPGA. The POET interface facilitates local switching among multiple fabric ports, allowing scalable mesh

Mercury Systems is a best-of-breed provider of commercially developed, open sensor and Big Data processing systems, software and services for critical commercial, defense and intelligence applications.













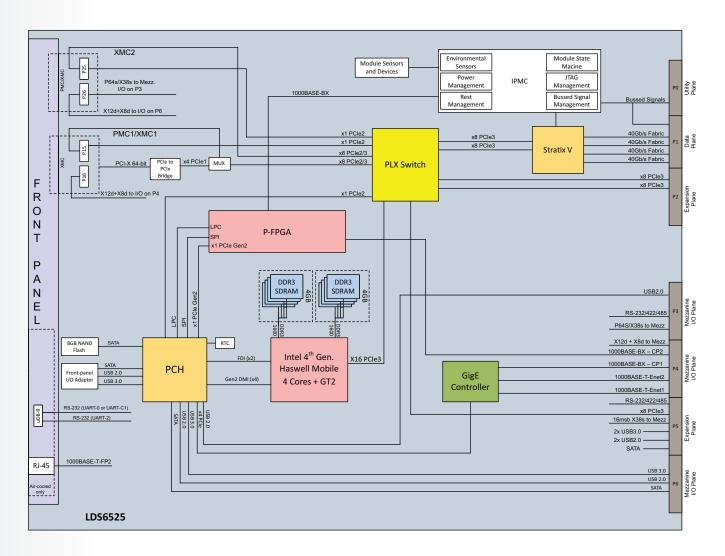


Figure 1. LDS6525 functional block diagram

and switching based subsystem designs. The open and downloadable nature of POET allows users of the LDS6525 to implement these different protocols on the OpenVPX data plane without hardware changes. Users can also integrate their custom IP with POET to enhance the value of their subsystems.

PCle Architecture

The LDS6525 provides single 81-lane Gen3 PCle switches for both on-board switching and off-board expansion. This switch complex provides an x8 PCle interface to each of the two XMC sites, as well as an x4 connection to a PCle to PCl-X* bridge for the single PMC site. This allows mezzanines to operate at full bandwidth, optimizing the flow of I/O into the processing subsystem.

Externally, the LDS6525 implements a full Gen3 x16 PCle connection to the OpenVPX expansion plane on the P2 VPX connector. This expansion plane interface enables the LDS6525's compatibility with Mercury's GPU or FPGA based co-processing modules. These configuration options let the module effectively act as an upstream/downstream PCle switch to allow the "chaining" of PCle devices.

Mezzanine Card Flexibility

The LDS6525 provides two mezzanine sites: one PMC/XMC and one XMC-only. Each of the standard mezzanine sites on the LDS6525 module can be configured with off-the-shelf mezzanine cards to bring additional I/O into the system for processing or control. PMC cards are supported with a 32-bit or 64-bit PCI/PCI-X interface at up to 133 MHz on the PMC/XMC site, with PMC user-defined I/O mapped to the backplane. XMCs are supported with x8 PCIe on the J15/J25 connector per the VITA 42.3 standard. There are 16 differential pairs and 38 single-ended signals of XMC user I/O mapped to the backplane via the J16/J26 connector.

The LDS6525 supports configuration with either VITA 42 or VITA 61 XMC connectors. Air-cooled variants are populated by default with the VITA 42 XMC connector, while rugged conduction-cooled or Air-Flow-By variants are populated by default with VITA 61 XMC connectors. The VITA 61 connector offers superior signal integrity characteristics and is a more rugged design, appropriate for high-end XMC modules utilizing Gen3 PCle interfaces in environmentally challenging applications.

Multiple I/O Options

In addition to the flexibility offered via the on-board mezzanine sites, the LDS6525 offers a variety of additional built-in I/O options:

- One 10/100/1000BASE-T Gigabit Ethernet connection can be routed to the front-panel on air-cooled configurations or to the backplane.
- One additional 10/100/1000BASE-T Gigabit Ethernet connection is routed to the backplane.
- Two 1000BASE-BX SERDES Ethernet connections are routed to the backplane per the OpenVPX control plane specification.
- One TIA-232 serial port is routed to the front-panel on air-cooled configurations, or to the backplane on conduction-cooled configurations. When routed to the backplane, the serial interface can be configured for either TIA-232 or TIA-422 signaling.
- One front-panel USB 3.0 interface is available on air-cooled configurations.
- Two backplane USB interfaces are available (one 2.0, one 3.0) with both air-cooled and conduction-cooled configurations.
- Two SATA interfaces to the backplane are provided to interface with storage devices.
- Eight GPIO lines act as discrete I/O usable as input, output, or to generate interrupts on the module.
- Several additional bused signals enhance the functionality of the LDS6525 module.

System Management

The LDS6525 module implements the advanced system management functionality architected in the OpenVPX specification to enable remote monitoring, alarm management, and hardware revision and health status. Using the standard I2C bus and Intelligent Platform Management Controller (IPMC) protocol, the on-board system management block implements the IPMC.

This allows the LDS6525 module to:

- Read sensor values
- Read and write sensor thresholds, allowing an application to react to thermal, voltage or current variations that exceed those thresholds
- Reset the entire module
- Power up/down the entire module
- Retrieve module Field Replaceable Unit (FRU) information
- Be managed remotely by a Chassis Management Controller at the system level, such as implemented on Mercury's 6U OpenVPX switched fabric modules

VPX-REDI

The VPX (VITA 46) standard defines 6U and 3U board formats with a modern high-performance connector set capable of supporting today's high-speed fabric interfaces. VPX is most attractive when paired with the Ruggedized Enhanced Design Implementation standard — REDI (VITA 48). The LDS6525 module is a 6U conduction-cooled/Air Flow-By $^{\text{TM}}$ implementation of VPX-REDI, with air-cooled variants in the same VPX form factor available for less rugged environments.

Targeted primarily for harsh-environment embedded applications, VPX-REDI offers extended mechanical configurations supporting higher functional density, such as two-level maintenance (2LM). 2LM allows maintenance personnel to replace a failed module and restore the system to an operational state in a limited time period.

Air Flow-By

Air-cooled chassis require filters to remove contaminants from their cooling air streams. Mercury's Air Flow-By technology eliminates filtration with the most elegant cooling solution available within a sealed and rugged package. Air Flow-By technology is resilient, boosts SWaP, reduces operating temperature, extends MTBF by an order of magnitude and enables the most powerful processing solutions.

Additional Features

The LDS6525 module provides all the features typically found on a single-board computer. In addition to the sophisticated management subsystem and switched fabric interconnect, the LDS6525 module provides users with a toolkit enabling many different application use cases. Features include:

- Real-time clock with granularity to 1 ms and time measurement of up to 30 years
- General-purpose timers for synchronization
- Watchdog timer to support processor interrupt or reset
- Multiple boot paths, including netboot, USB boot and boot from SATA or the on-board 8 GB flash device.

Open Software Environment

Mercury leverages over 30 years of multicomputer software expertise, including recent multicore processor expertise, across its many platforms. This strategy is fully applied to the LDS6525 module. The same Linux® development and run-time environment is implemented on the LDS6525 module as on other Intel-based Mercury platforms across the Ensemble 3000, 5000 and 6000 Series. Off-the-shelf open software such as OFED, OpenMPI and MultiCore Plus™ are fully supported by the POET enabled data plane.

Open Standards Mean Interoperability and Planning for the Future

The OpenVPX/VITA 65 standard is an industry initiative launched by defense prime contractors and COTS commercial system developers to take a proactive approach to solving the interoperability issues associated with the VITA 46 (VPX) family of specifications. This group has created an overarching System Specification defining VPX system architecture through pinout definitions to establish a limited set of application-specific reference solutions. These OpenVPX standard solutions provide clear design guidance to COTS suppliers and the user community, assuring interoperability across multi-vendor implementations. The OpenVPX System Specification was ratified by the VSO in February 2010, and it was ANSI approved as the VITA 65 standard in July 2010.

Specifications

Processor

Single 2.4GHz 4th Generation Intel i7 Quad-Core mobile (Haswell mobile) CPU (i7-4700EQ)

Threads per core: 2 (8 total per CPU)

On-die GT2 GPU

Processor support: AVX2, 256 bit vector engine incorporating

Fused Multiple-Add (FMA)
Peak performance per module:

Processor: 307 GFLOPS GT2 GPU: 208 GFLOPS

PCle Gen 3 (x8)

OpenCL

PCH (Platform Controller Hub) LynxPoint mobile QM87

Intelligent Platform Management Interface (IPMI)

On-board IPMI controller

Voltage and temperature monitor

Geographical address monitor

Power/reset control

On-board FRU EEPROM interface

FPGA, CPU and CPLD interfaces

Ethernet Connections

1000BASE-BX Ethernet to P4 connector

OpenVPX control plane

10/100/1000BASE-T Ethernet to P4 connector

Accessible via OpenVPX RTM or external chassis interface

10/100/1000BASE-T Ethernet connection

To front-panel (air-cooled module) or backplane P4 connector (conduction-cooled module)

Control plane functions supported by the chipset include:

UDP, TCP, SCTP, ARP, IPv4, IPv6, IEEE1588, flow control, 802.1P (priority) and 802.1Q (VLAN)

OpenVPX Multi-Plane Architecture

System management via IPMB-A and IPMB-B links on P0 management plane Gen 2 Serial RapidIO or 10 Gigabit Ethernet interfaces on P1 data plane Full x16 or dual x8 Gen3 PCle expansion plane to P2 connector Dual 1000BASE-BX Ethernet control plane

PMC/XMC Sites

Mezzanine sites 1 PMC/XMC and 1 XMC

PCI-X to PCIe bridge Connects PMC site to on-board

PCle

PMC PCI support 33 and 66 MHz

PMC PCI-X support 66, 100, and 133 MHz

PMC user-defined I/O from J14 to backplane

PCIe XMC sites per VITA 42.3 with XMC user-defined I/O from Jn6 to backplane

Additional I/O Capabilities

One RS-232 serial interface to front-panel (air-cooled) or backplane (conduction-cooled)

Configurable for RS-232 or RS-422 signaling when routed to backplane

One additional RS-232/RS-422 serial interface to backplane

One front-panel USB 3.0 interface (air-cooled configurations only)

One USB 2.0 interface to backplane

One USB 3.0 interface to backplane

One DVI interface to backplane

Two SATA interfaces to backplane

Eight single-ended GPIO interfaces to backplane

System signals to backplane

NVMRO, Chassis Test, Environmental Bypass, Memory Clear

Mechanical

6U OpenVPX

1.0" slot pitch

OpenVPX and VPX-REDI

Compliance

OpenVPX system standard encompasses VITA 46.0, 46.3, 46.4, 46.6, 46.11

Compatible with VITA 65

VITA 46/48.1/48.2 (REDI)

Serial RapidIO, PCIe, 10 Gigabit Ethernet

Environmental

		Air-cooled Air-cooled			Conduction-cooled
		Commercial (L0)	Rugged (L1)	Air Flow-By (Rugged L4)	Rugged (L3)
Ruggedness		•	• •	•••	•••
Moisture/dust protection		•	••	•••	•••
Typical cooling performance		~170W*	~150W*	~250W*	~150W**
Temperature	Operating*	-0°C to +40°C	-25°C to +55°C	-40°C to +55°C	-40°C to +71°C
	Storage	-40°C to +85°C	-55°C to +85°C	-55°C to +125°C	-55°C to +125°C
Operating temperatures rate of change		N/A	5°C/min	10°C/min	10°C/min
Humidity	Operating*	10-90%, non-condensing	5-95%, non-condensing	5-95%, non-condensing 100% condensing	5-95%, non-condensing 100% condensing
	Storage	10-90%, non-condensing	5-95%, non-condensing	5-95%, non-condensing 100% condensing	5-95%, non-condensing 100% condensing
Altitude	Operating*	0-10,000ft	0-30,000ft	0-30,000ft	0-70,000ft
	Storage	0-30,000ft	0-50,000ft	0-100,000ft	0-100,000ft
Vibration	Random	0.003 g²/Hz; 20-2000 Hz, 1 hr/axis	0.04 g²/Hz; 20-2000 Hz, 1 hr/axis	0.10 g²/Hz; 5-2000 Hz, 1 hr/axis	0.1 g²/Hz; 5-2000 Hz, 1 hr/axis
	Sine	N/A	N/A	10G peak; 5-2000 Hz, 1 hr/axis	10G peak; 5-2000 Hz, 1 hr/axis
		z-axis: 20g;	z-axis: 50g;	z-axis: 50g;	z-axis: 50g;
	Shock	x and y-axes: 32g; (11ms 1/2-sine pulse,	x and y-axes: 80g; (11ms 1/2-sine pulse,	x and y-axes: 80g; (11ms 1/2-sine pulse,	x and y-axes: 80g; (11ms 1/2-sine pulse,
		3 positive, 3 negative)			
Salt/Fog		N/A	Contact Factory	Designed to 10% NaCl	Designed to 10% NaCl

^{*} Customer must maintain required cfm level

All products manufactured by Mercury meet elements of the following specifications: All products manufactured by Mercury meet elements of the following specifications: MIL-Q-9858A, MIL-E-5400T, MIL-STD-454M, MIL-STD-45662A, MIL-STD-275E, MIL-STD-883C, MIL-HDBK-217F, MIL-STD-2036 and MIL-I-46058C, and various IPC standards. Mercury's inspection system has been certified in accordance with MIL-I-45208A.



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^{**} Card edge should be maintained below 71°C